Ordering number : EN4476B

Monolithic Digital IC





LB1854M

Three-Phase Brushless Motor Driver IC

Overview

The LB1854M is a three-phase brushless motor driver IC and is optimal, in particular, for driving VCR capstan and drum motors.

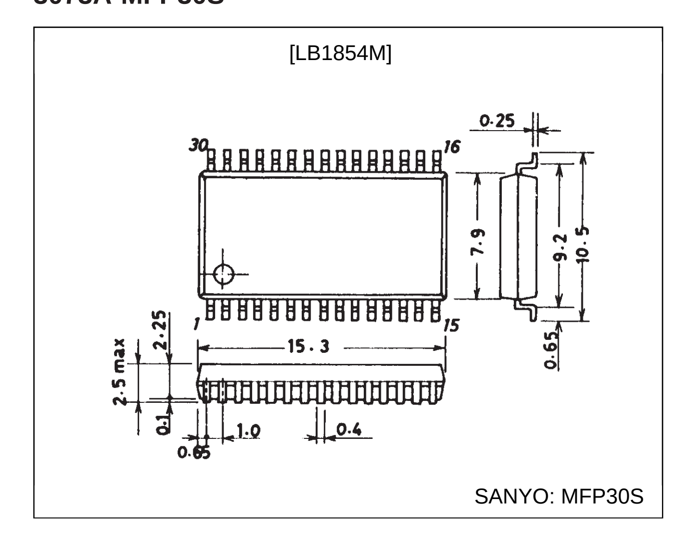
Features

- 120° voltage linear drive technique
- The LB1854M soft switching scheme allows smaller external capacitors to be used (e.g., chip capacitors).
- Built-in thermal-shutdown function
- Built-in overcurrent protection circuit
- Built-in FG amplifiers (operational amplifier and Schmitt amplifier)
- Control start voltage set by an external voltage
- The output current feedback level can be changed by changing the control gain to one of two levels.

Package Dimensions

unit: mm

3073A-MFP30S



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}1$ max		20	V
	$V_{CC}2$ max		7.0	V
Applied output voltage	$V_{OU, V, W}$		22	V
Maximum output current	I_{OUT} max		1.5	A
Allowable power dissipation	Pd max		1.05	W
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–55 to +150	°C

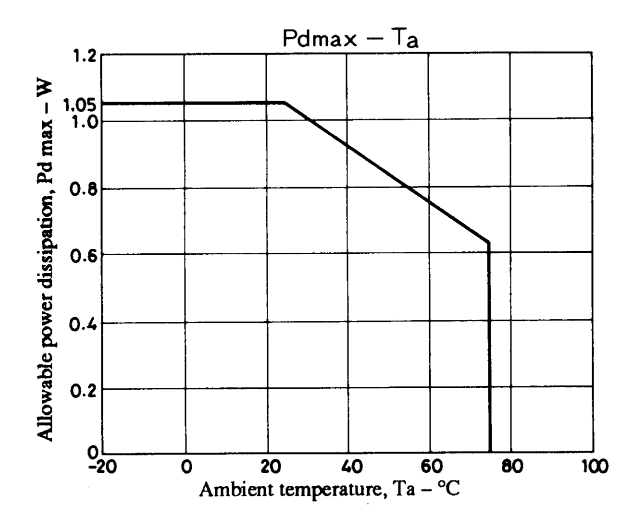
Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}1$		5 to 18	V
	$V_{CC}2$		4.3 to 6.5	V

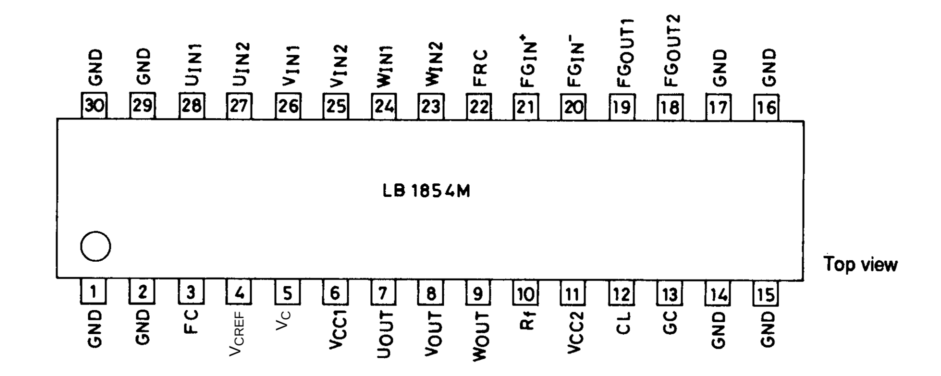
Electrical Characteristics at Ta = 25°C, $V_{CC}1$ = 12 V, $V_{CC}2$ = 5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain	$I_{CC}1$	V_C = 0 V, R_L = ∞		17	30	mA
	$I_{CC}2$	V_C = 0 V		6.5	9.5	mA
[Drive Block]						
Output saturation voltage	V_O (sat) 1	I_{OUT} = 0.5 A, sink + source		1.6	2.2	V
	V_O (sat) 2	I_{OUT} = 1.0 A, sink + source		2.0	3.0	V
Output TRS breakdown voltage	V_O (sus)	I_{OUT} = 20 mA*	20			V
Output resting potential	V_{OQ}	V_C = 0 V	5.7	6.0	6.3	V
Hall amplifier input offset voltage	V_H offset		–5		+5	mV
Hall amplifier input bias current	I_H bias			1	5	µA
Hall amplifier common mode input voltage range	V_H ch		1.3		2.2	V
Hall input/output voltage gain	GV_{HO}		43	46	49	dB
[Control Block]						
Control output drive gain	$GV_{CO}1$	High gain	37	40	43	dB
	$GV_{CO}2$	Low gain	31	34	37	dB
Control output CH difference	ΔGV_{CO}		–2		+2	dB
Control start voltage	V_{CTH}	When V_{OUT}p-p = 2 V		2.5		V
Gain control switching high level			4		5	V
Gain control switching middle level		Middle level when the input is open	2		3	V
Gain control switching low level			0		1	V
[FG Amplifier]						
FG amplifier input offset voltage	V_{FG} offset		–8		+8	mV
Open-loop voltage gain	GV_{FG}	f = 1 kHz		60		dB
Source output saturation voltage	$V_{FG\ OU}$	I_O = 2 mA	37			V
Sink output saturation voltage	$V_{FG\ OD}$	I_O = –2 mA			1.3	V
Common-mode signal rejection ratio	CHR	*		80		dB
FG amplifier common-mode input voltage range	$V_{FG\ CH}$		0		3.5	V
Phase margin		*		20		Deg
Schmitt hysteresis	ΔVsh1	$FG_{OUT}2$: High to low		22		mV
	ΔVsh2	$FG_{OUT}2$: Low to high		22		mV
Schmitt input voltage range	Vsh_{CH}		0.7		3.5	V
[Thermal Shutdown]						
Operating temperature	TSD	*	150	180	210	°C
Hysteresis	ΔTSD	*		15		°C

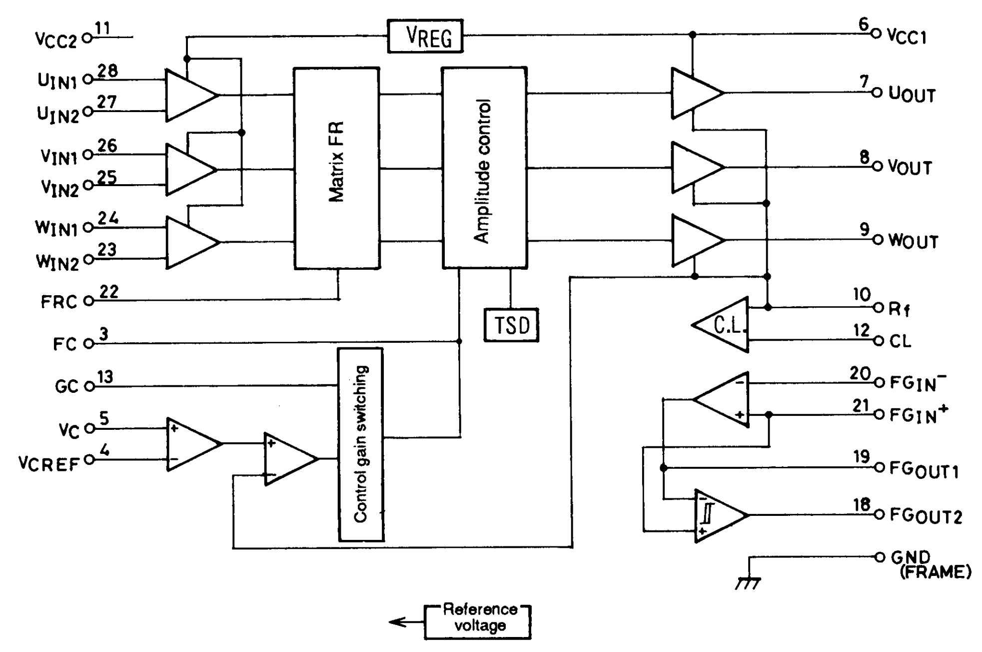
Note: * Items marked with an asterisk are design target values and are not measured.



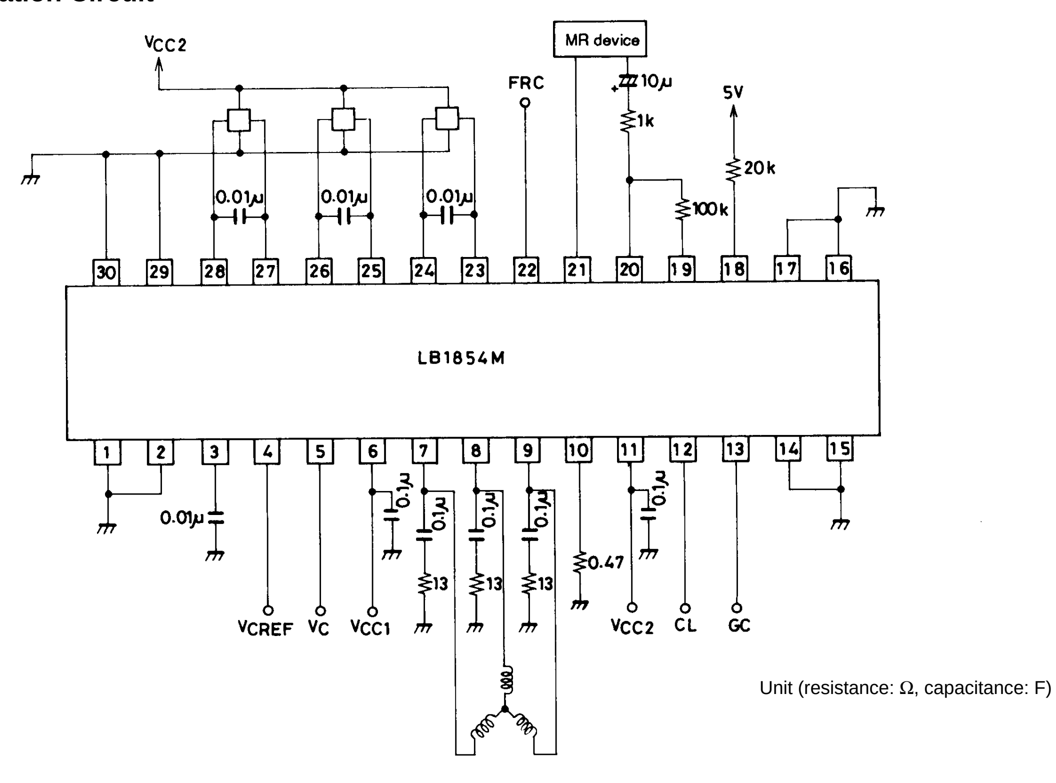
Pin Assignment



Block Diagram



Sample Application Circuit



Unit (resistance: Ω, capacitance: F)

Truth Table

	Source / Sink	Input			Forward and reverse control F/RC
		U	V	W	
1	W phase → V phase	H	H	L	L
	V phase → W phase				H
2	W phase → U phase	H	L	L	L
	U phase → W phase				H
3	V phase → W phase	L	L	H	L
	W phase → V phase				H
4	U phase → V phase	L	H	L	L
	V phase → U phase				H
5	V phase → U phase	H	L	H	L
	U phase → V phase				H
6	U phase → W phase	L	H	H	L
	W phase → U phase				H

Input high: Phase 1 is 0.2 V or more higher than the corresponding phase 2 for each phase input.
Low: Phase 1 is 0.2 V or more lower than the corresponding phase 2 for each phase input.
Forward and reverse control high: 2.3 V to $V_{CC}1$
Low: 0 V to 0.7 V

Pin Functions

Unit (resistance: Ω)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Function
1, 2, 14, 15, 16, 17, 29, 30	FRAME (GND)			Ground for all circuits except the outputs
3	FC			The gain frequency characteristics can be lowered by connecting a capacitor between this pin and ground to prevent oscillation.
4 5	$V_{C\ REF}$ V_C	1.5 V min $V_{CC}2$ max 0 V min $V_{CC}2$ max		Speed control The LB1854M implements a voltage control scheme in which the output voltage is controlled by the pin 5 voltage. The pin 4 voltage determines the control start voltage.
6	$V_{CC}1$	5 to 18 V		Power supply that provides the drive outputs

Continued from preceding page.

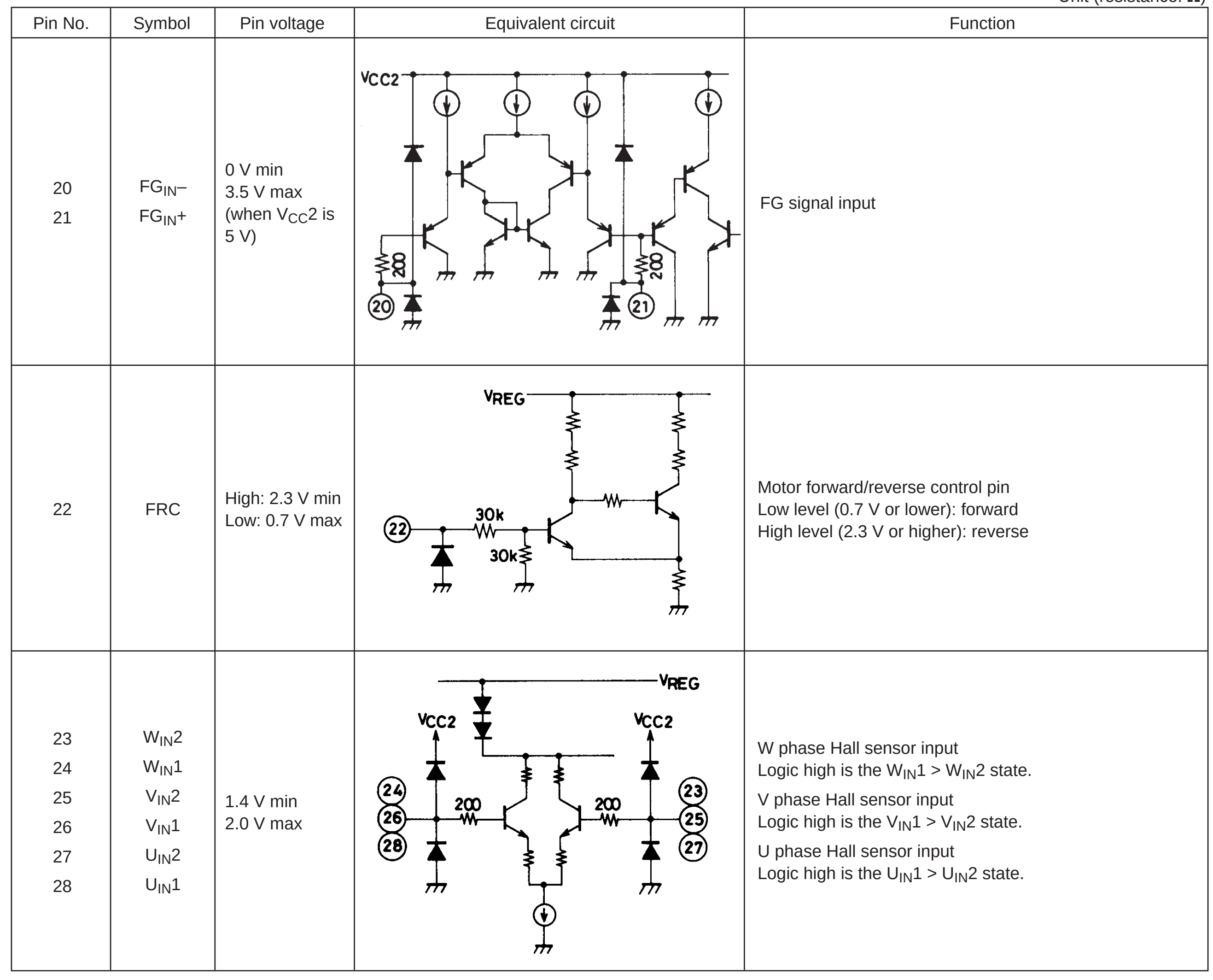
Unit (resistance: Ω)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Function
7 8 9	U_{OUT} V_{OUT} W_{OUT}			Output pins
10	R_f			Output transistor ground Feedback can be applied to the control amplifier by inserting resistor between this pin and GND and detecting the output current as a voltage. The overcurrent protection circuit (current limiter) operates by detecting the voltage on this pin.
11	$V_{CC}2$	4.3 to 6.5 V		Power supply provided to all blocks other than the output block This voltage must be stabilized so that no ripple or other noise is present.
12	CL	0 V min $V_{CC}2$ max		The current limiter operates when the R_f pin reaches the same potential as pin 12. The pin 12 potential is set up externally.
13	GC	0 V min $V_{CC}2$ max		Control input to output gain switching pin High level (4 to 5 V): 34 dB Middle level (2 to 3 V) or open: 40 dB (low speed): 34 dB (high speed) Low level (0 to 1 V): 40 dB However, note that this applies when $V_{CC}2$ is 5 V.
18	$FG_{OUT}2$			FG Schmitt amplifier output
19	$FG_{OUT}1$			FG amplifier output

Continued on next page.

Continued from preceding page.

Unit (resistance: Ω)



Pin No.	Symbol	Pin voltage	Equivalent circuit	Function
20 21	$FG_{IN}-$ $FG_{IN}+$	0 V min 3.5 V max (when $V_{CC}2$ is 5 V)		FG signal input
22	FRC	High: 2.3 V min Low: 0.7 V max		Motor forward/reverse control pin Low level (0.7 V or lower): forward High level (2.3 V or higher): reverse
23 24 25 26 27 28	$W_{IN}2$ $W_{IN}1$ $V_{IN}2$ $V_{IN}1$ $U_{IN}2$ $U_{IN}1$	1.4 V min 2.0 V max		W phase Hall sensor input Logic high is the $W_{IN}1 > W_{IN}2$ state. V phase Hall sensor input Logic high is the $V_{IN}1 > V_{IN}2$ state. U phase Hall sensor input Logic high is the $U_{IN}1 > U_{IN}2$ state.